

Model Name:GA-P41T-D3P Revision 1.6

SHEET TITLE

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02	BLOCK DIAGRAM
03	BOM & PCB MODIFY HISTORY
04	P4_LGA775_A
05	P4_LGA775_B,D
06	P4_LGA775_C
07	P4_LGA775_E,F,G,H
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09	Eaglelake DDR
10	Eaglelake PCI_EXP_16,DMI
11	Eaglelake VGA
12	Eaglelake GND
13	Eaglelake PWR
14	PCI EXPRESS*16 SLOT
15	DDRII CHANNEL A
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17	DDRII TERMINATION
18	ICH7 PCI, USB, DMI, LAN
19	ICH7 IDE, GPIO, SATA, CTRL
20	ICH7 VCC, GND
21	CK505 CLOCK.
22	PCI SLOT 1,2,PCIE*1
23	IDE/FLOPPY
24	ITE 8718 GB/HX
25	COM_LPT
26	CI,HWM,KB/MS,DUAL BIOS
27	ALC888

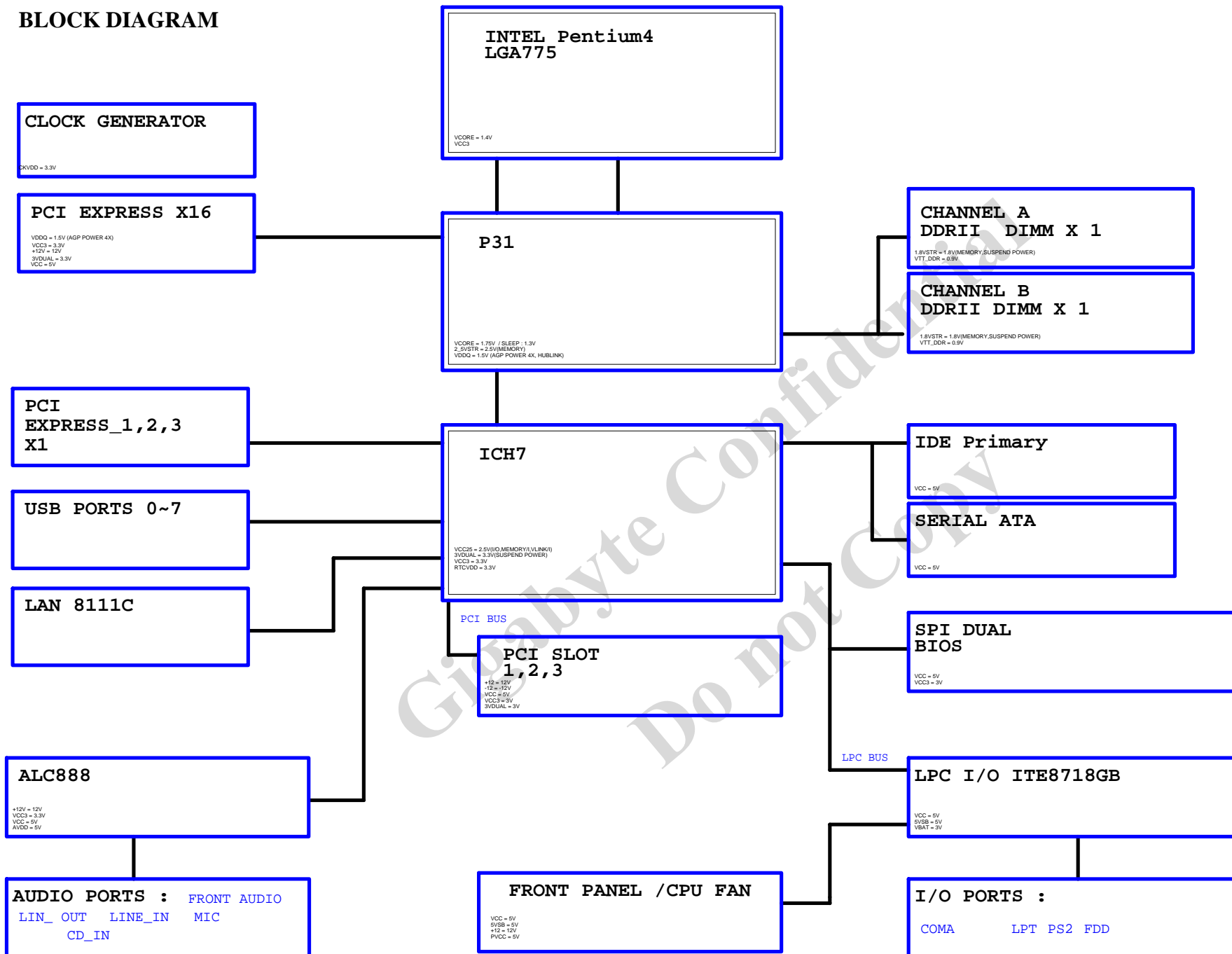
SHEET TITLE

28	REAR AUDIO JACK
29	DISCRETE POWER
30	VCORE PWM_ISL6312
31	ATX, OTHERS POWER
32	FRONT PANEL
33	REALTEK RTL8111D
34	PCI SLOT3,PCIE*2,3

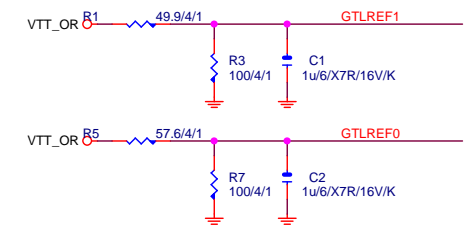
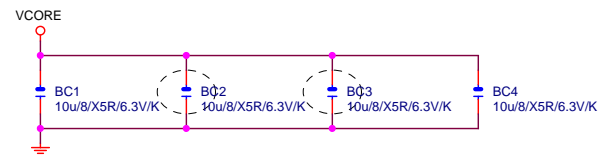
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Cover Sheet		
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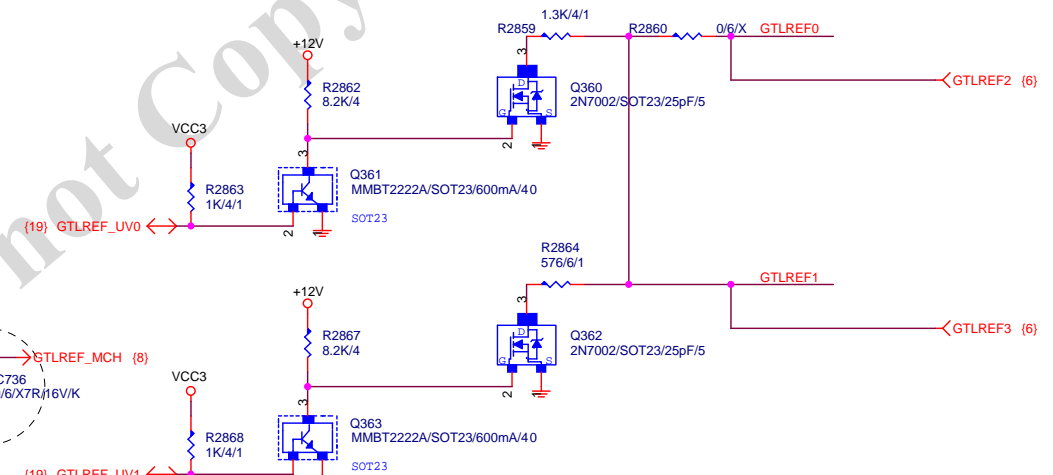
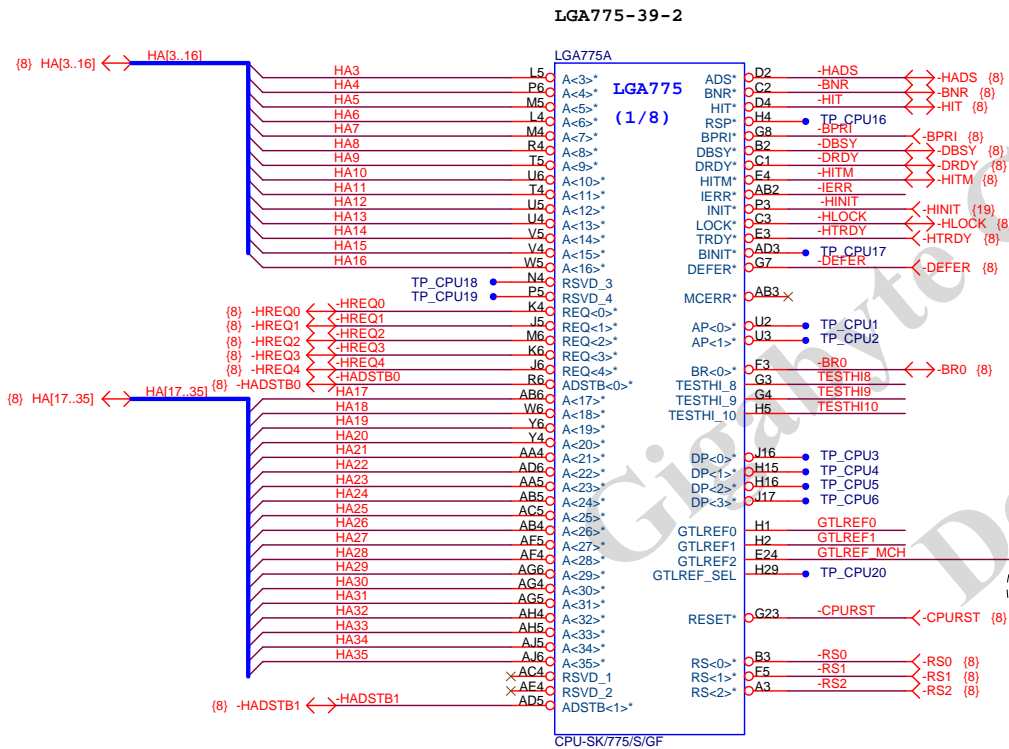
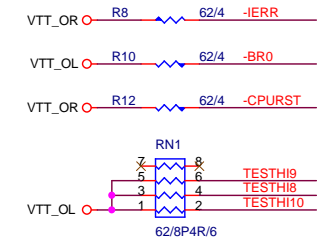
BLOCK DIAGRAM

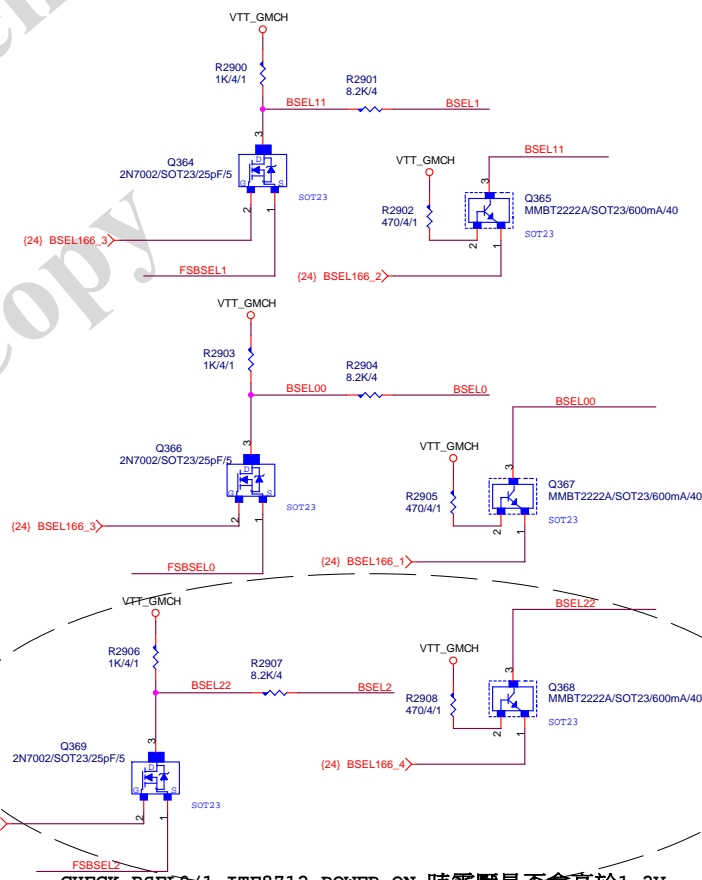
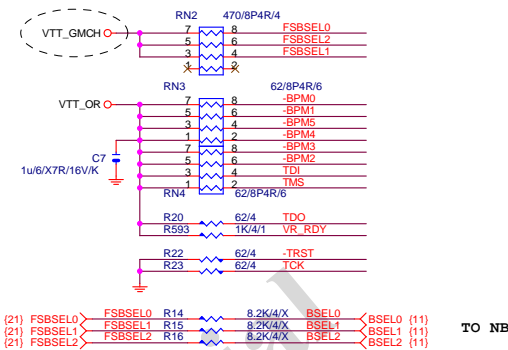


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BOM & PCB MODIFY HISTORY			
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中間値0.9V

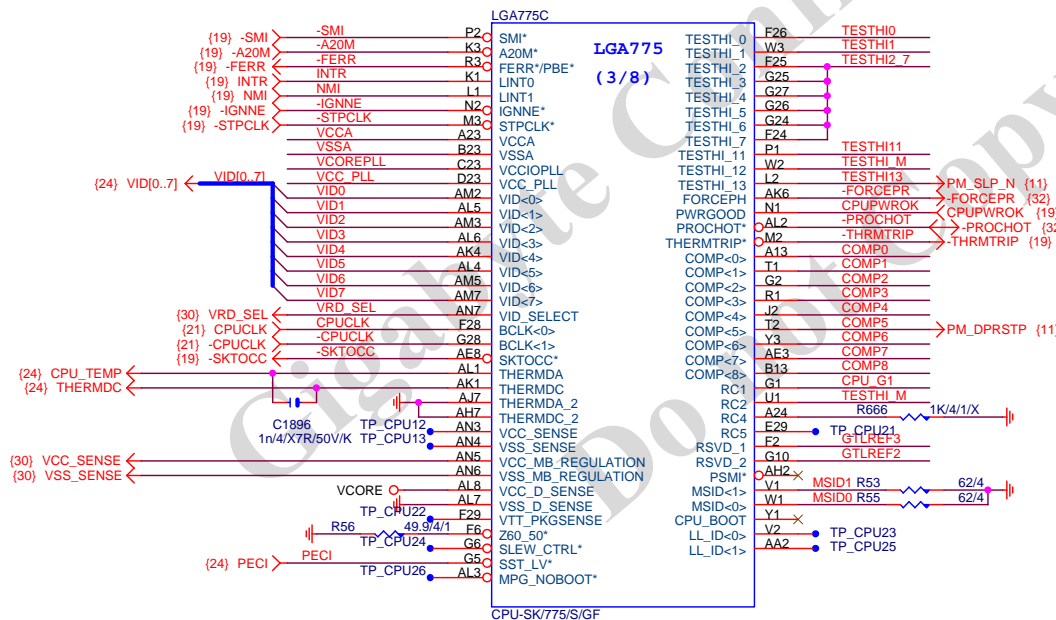
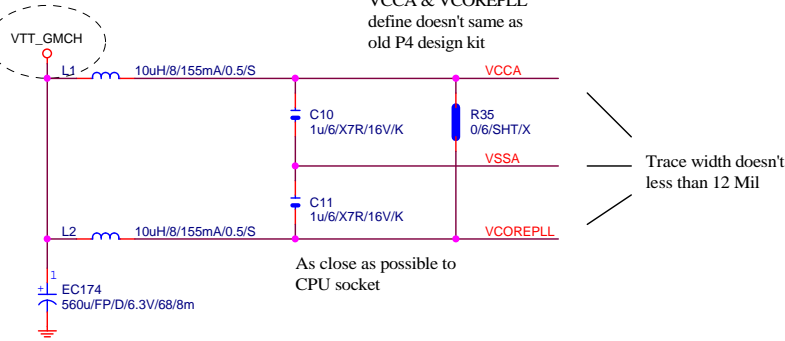




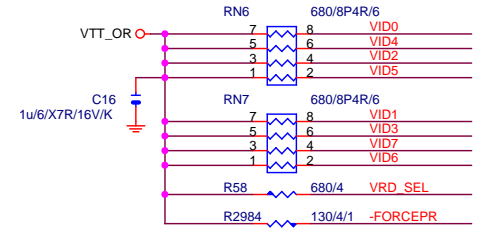
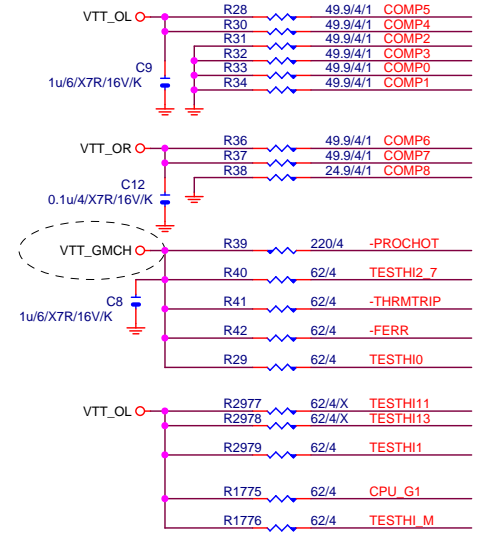
<i>Gigabyte Technology</i>			
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P4_LGA775-B,D			
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FSA	F5B	F5C			
F5BSEL0	F5BSEL1	F5BSEL2	Clock		
1	0	1	100MHz		
1	0	0	133MHz	3/4	400/533
0	1	0	200MHz	2/2.66/3.33/4	400/533/667/800
0	0	0	266MHz	2/2.5/3/4	533/667/800/1066
		1	333MHz	2/2.4	667/800
0	1	1	400MHz		

Note:
VCCA & VCOREPLL
define doesn't same as
old P4 design kit



Place outside of CPU socket



GTLREF3 → GTLREF3 (4)

GTLREF2 → GTLREF2 (4)



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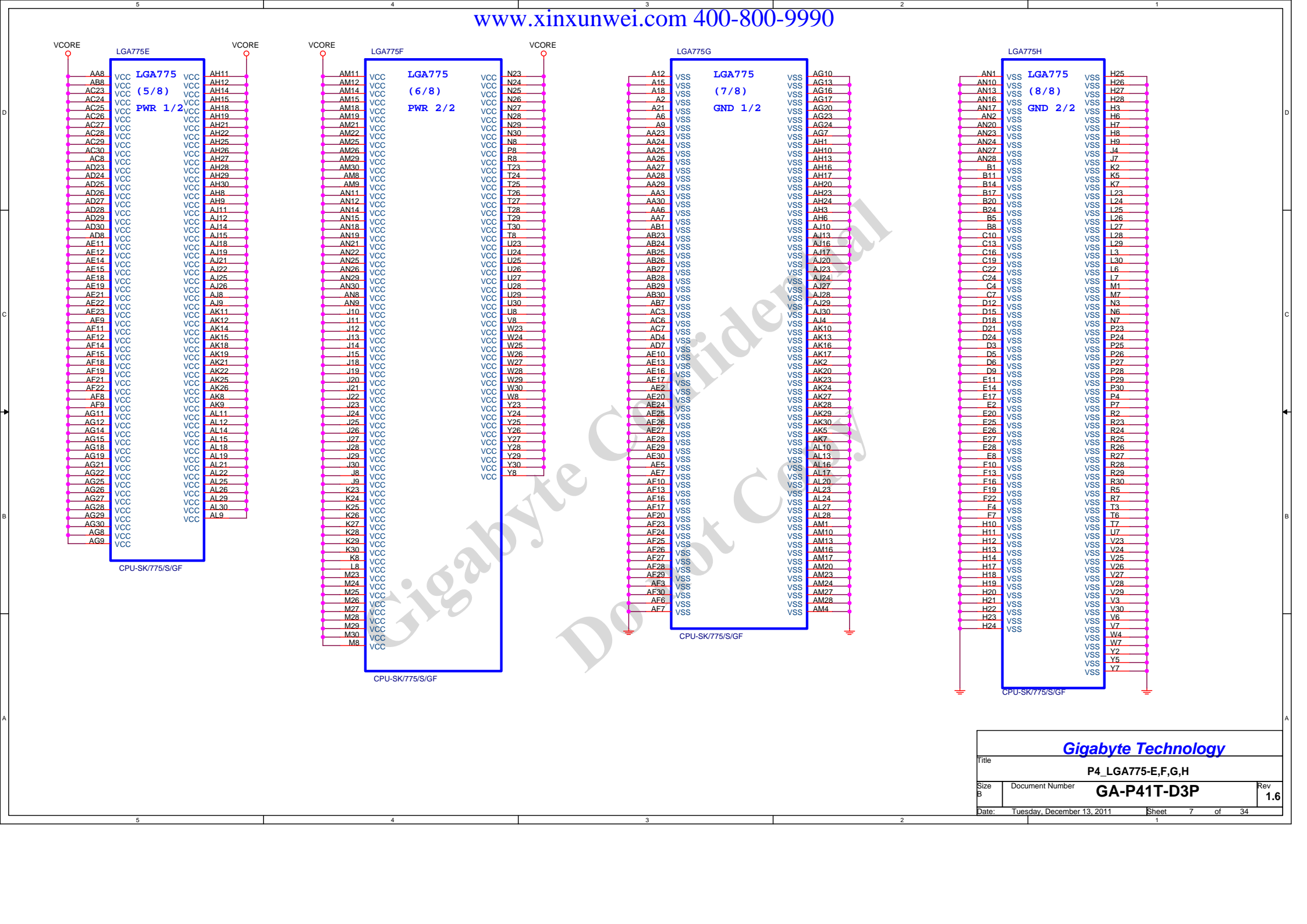
P4_LGA775-C

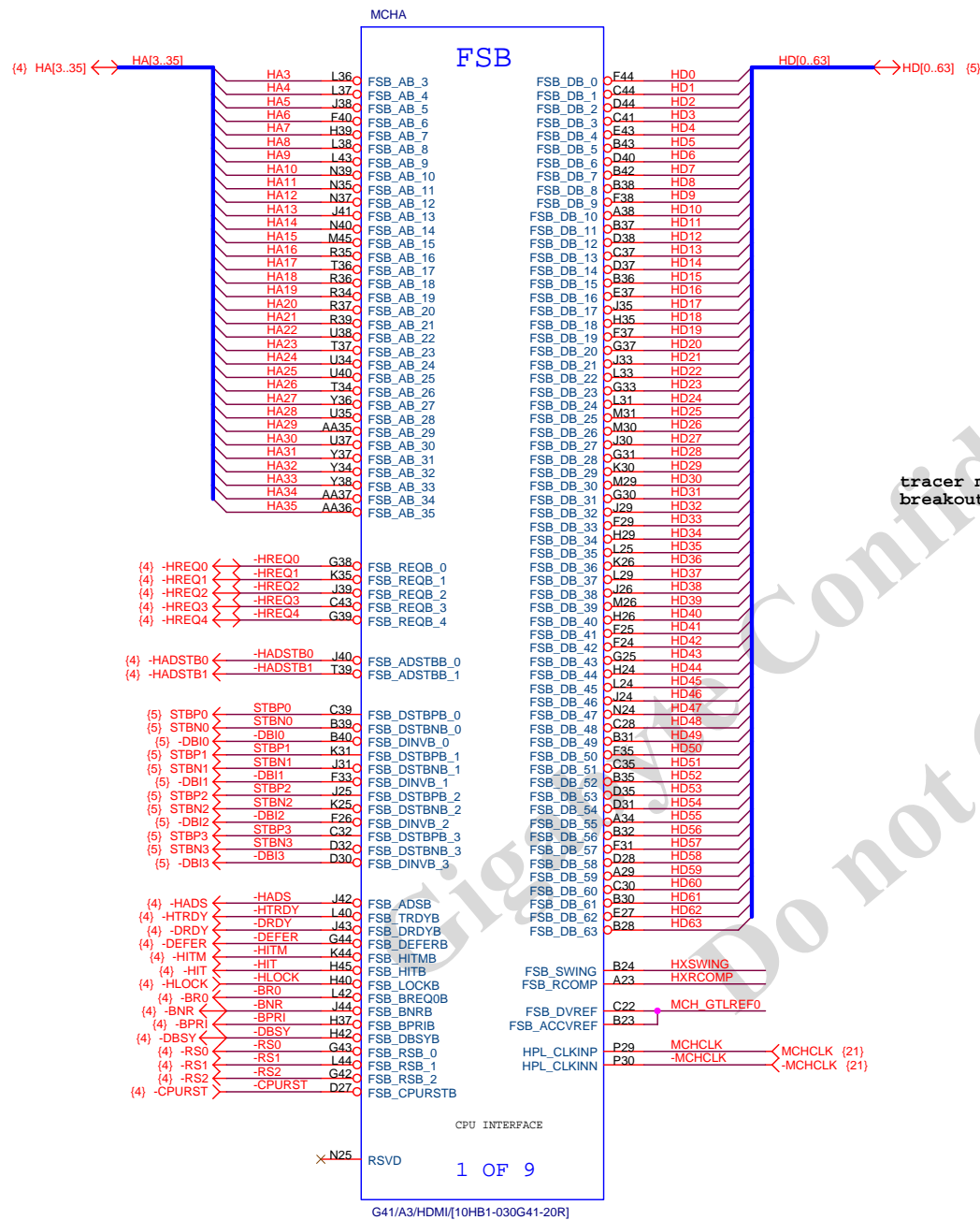
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PECI:Platform Environment Control Interface

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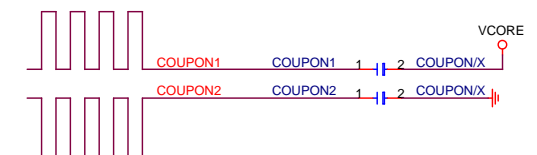


Not used for Core™2 Duo and Wolfdale

Note

tracer min 10/10 or (10/5
breakout), L1<3"

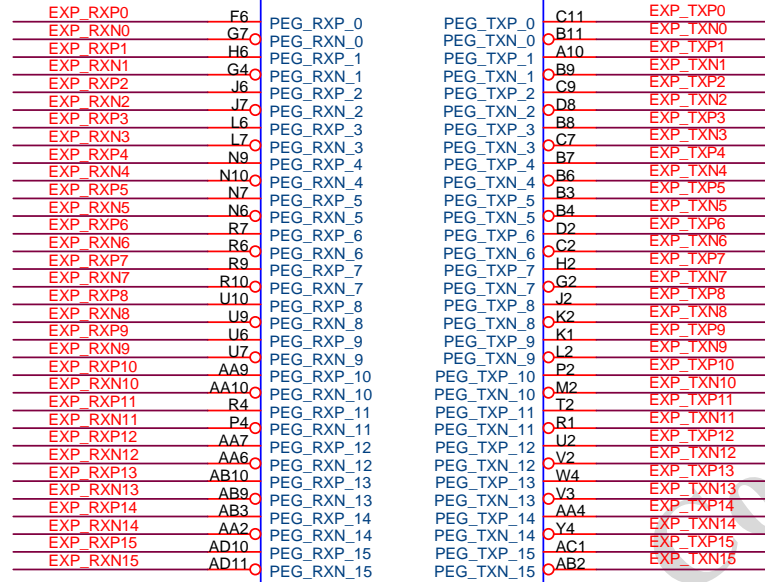
tracer 10/7 or
5/5(breakout)





PCIE16:16/5/5/5/16(breakout min 8/4/5/4/8)

Impedance=85 +/- 17.5%

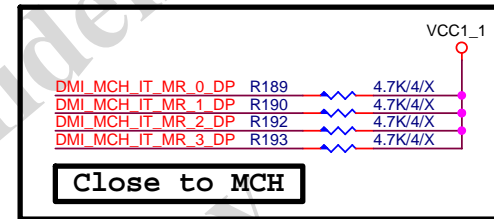
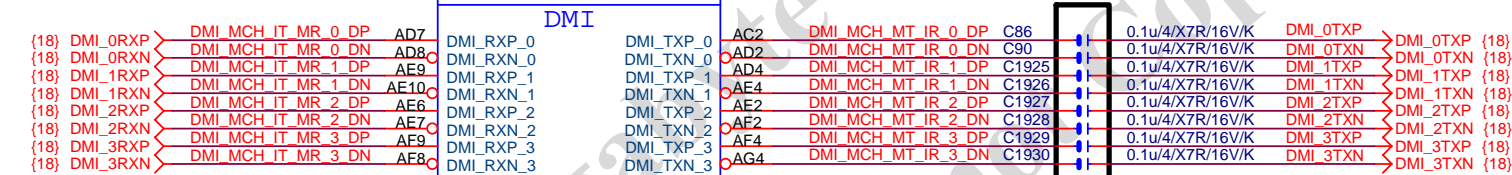


EXP_TXP[0..15] >> EXP_TXP[0..15] {14}

EXP_TXN[0..15] >> EXP_TXN[0..15] {14}

EXP_RXP[0..15] >> EXP_RXP[0..15] {14}

EXP_RXN[0..15] >> EXP_RXN[0..15] {14}

DMI:12/4/8/4/12
Impedance=95 +/- 17.5%

(21) SRCCLK_MCH >> SRCCLK_MCH D9

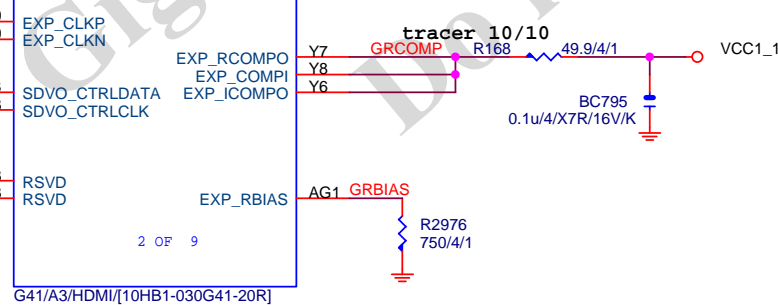
(21) -SRCCLK_MCH >> -SRCCLK_MCH E9

(14) SDVO_CLDATA >> SDVO_CLDATA J13

(14) SDVO_CLCLK >> SDVO_CLCLK G13

TP46 AB13

TP47 AD13



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GMCH-PCI E & DMI			
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EXP_SM

0:SDVO OR PCIE

1:BOTH SDVO AND

PCIE

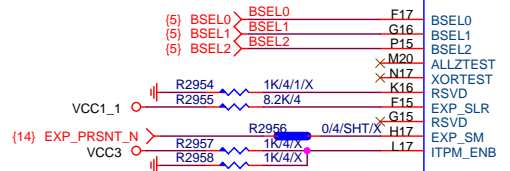
EXP_SLR:

0:BTX PCIE are reversed

1:ATX PCIE normal

MCHE

4/10//15<500 MILS



VGA

MISC

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G41/A3/HDMI/[10HB1-030G41-20R]

1th RGB:7.5/6 < 300 MILS

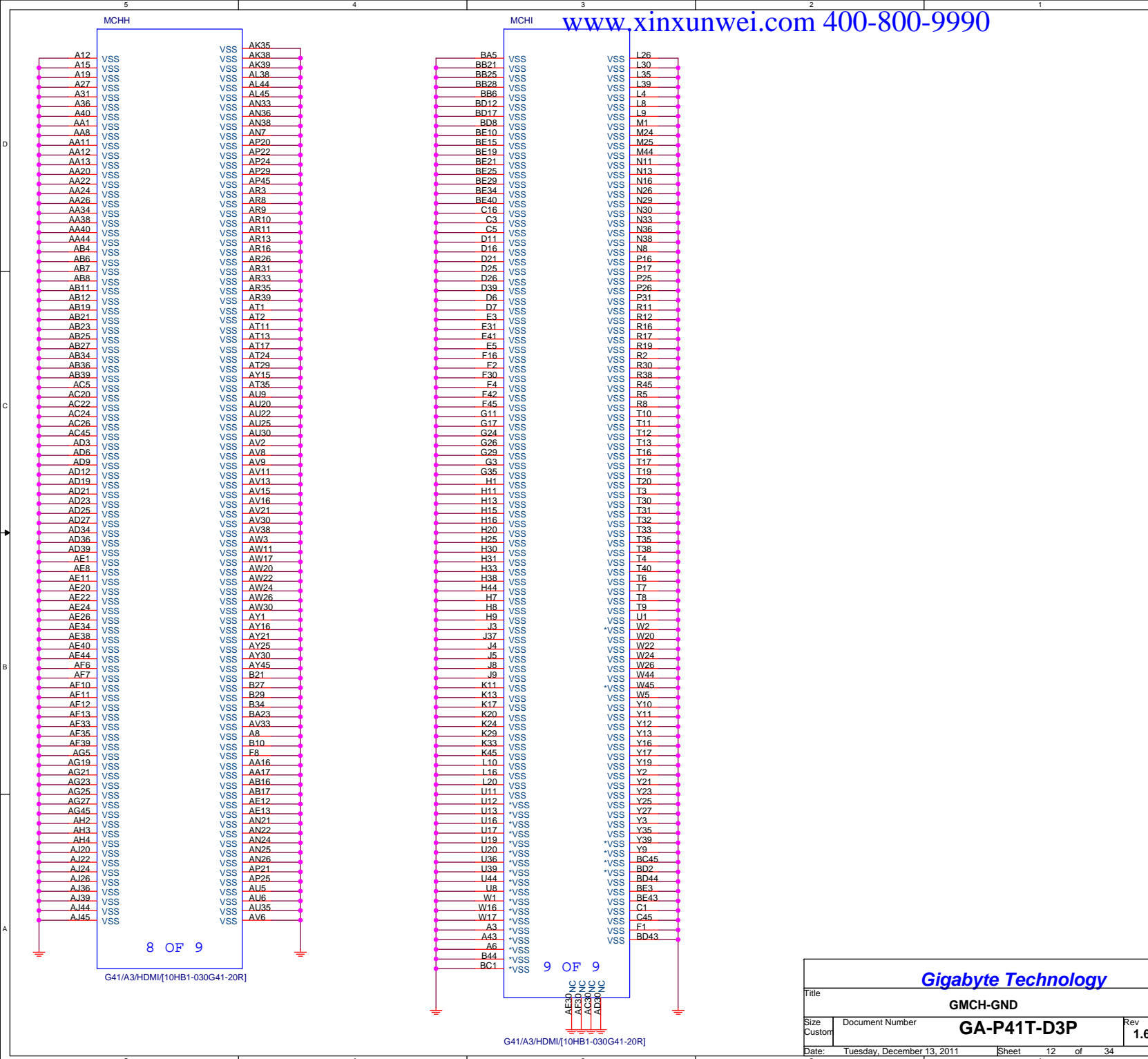
2th RGB:4/20 <5"~8" inch

ON-BOARD VGA 75ohm
non-ON-BOARD VGA 0ohmON-BOARD VGA 1.02k
non-ON-BOARD VGA 0ohmBW+ICH8 不要上(SAMPLE)
BW+ICH7 要上

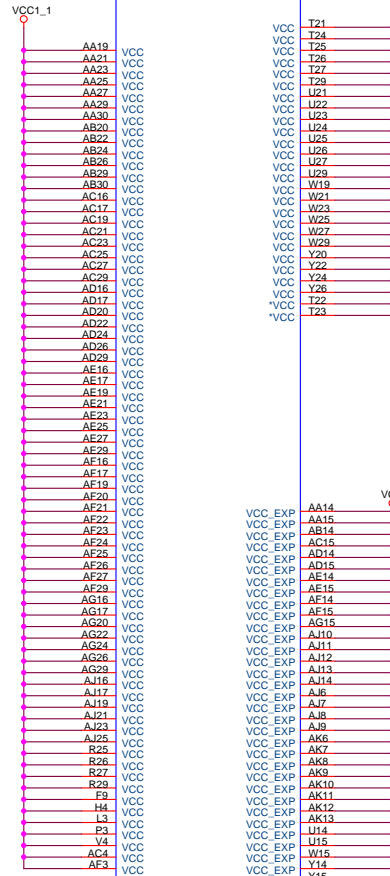
G41CHIP 都要上

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POWER

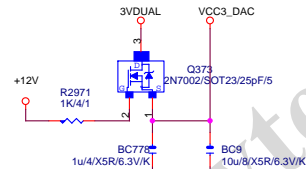


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G41/A3/HDMI[10HB1-030G41-20R]

CLOSE北橋 (注意震盪水波紋)

VCC3_DAC



VCC3_DAC

VCC3_DAC

VCC3_DAC

VCC3_DAC

VCC3_DAC

VCC3_DAC

VCC3_DAC

VCC3_DAC

VCC3_DAC

VCC3_DAC

VCC3_DAC

VCC3_DAC

VCC3_DAC

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VCC3_DAC

VCC3_DAC

VCC3_DAC

VCC3_DAC

VCC3_DAC

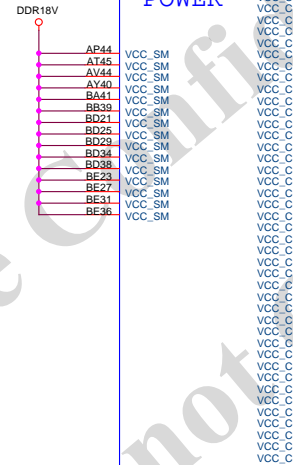
VCC3_DAC

VCC3_DAC

VCC3_DAC

VCC3_DAC

POWER



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G41/A3/HDMI[10HB1-030G41-20R]

VCC1_1

VCC1_1

VCC1_1

VCC1_1

VCC1_1

VCC1_1

VCC1_1

VCC1_1

VCC1_1

VCC1_1

VCC1_1

VCC1_1

VCC1_1

VCC1_1

VCC1_1

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VCC1_1

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VCC1_1

VCC1_1

VCC1_1

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VCC1_1

VCC1_1

VCC1_1

VCC1_1

VCC1_1

VCC1_1

VCC1_1

VCC1_1

VCC1_1

VCC1_1

VCC1_1

VCC1_1

VCC1_1

VCC1_1

VCC1_1

VCC1_1

VCC1_1

請考慮是否將短路移除

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GMCH-PWR

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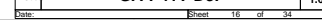


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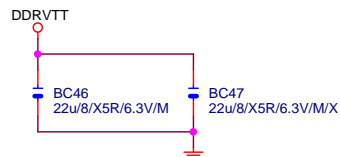
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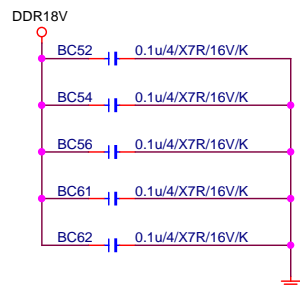


DDR TERMINATION CHANNEL A

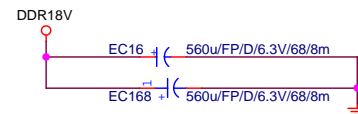
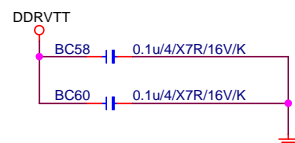
DDRVTT Decouple



DDR18V Decouple

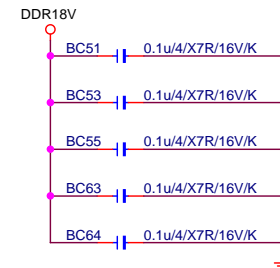


DDRVTT Decouple

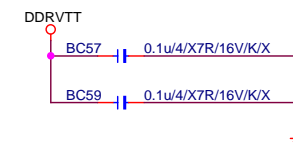


DDR TERMINATION CHANNEL B

DDR18V Decouple



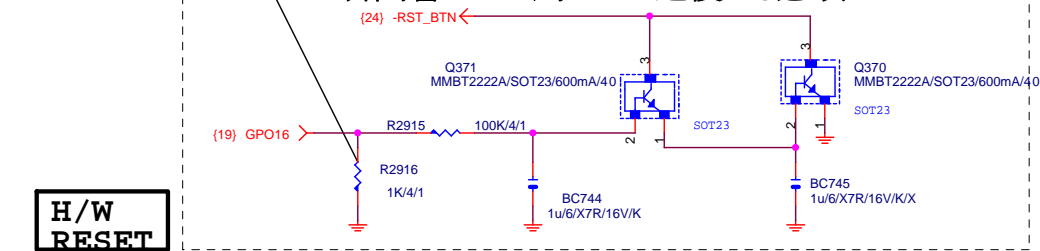
DDRVTT Decouple



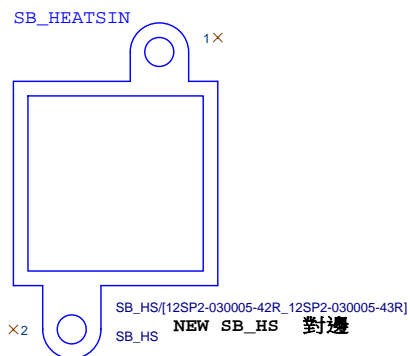
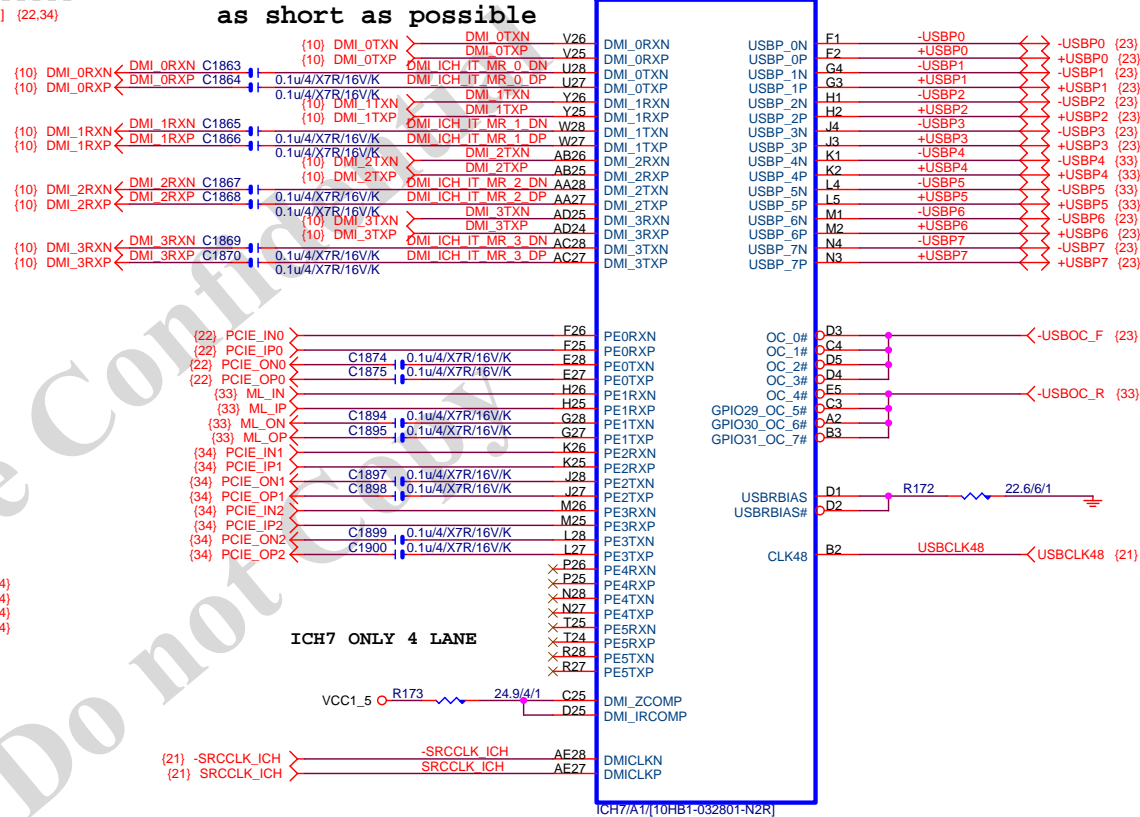
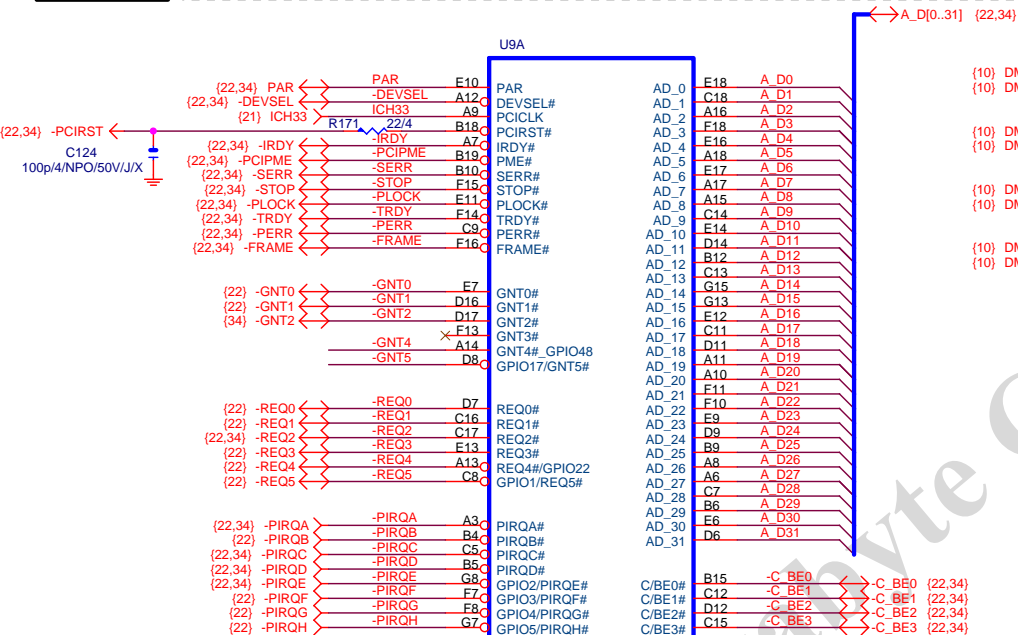
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FOR ICH7R POWER ON 瞬間會HIGH 到1.8V 之後0V,必須PULL DOWN 1K/6



Close to ICH
as short as possible



01=SPI
10=PCI
11=LPC (DEFAULT)



-GNT4 R1744 1K/4/1/X
-GNT5 R1745 1K/4/1

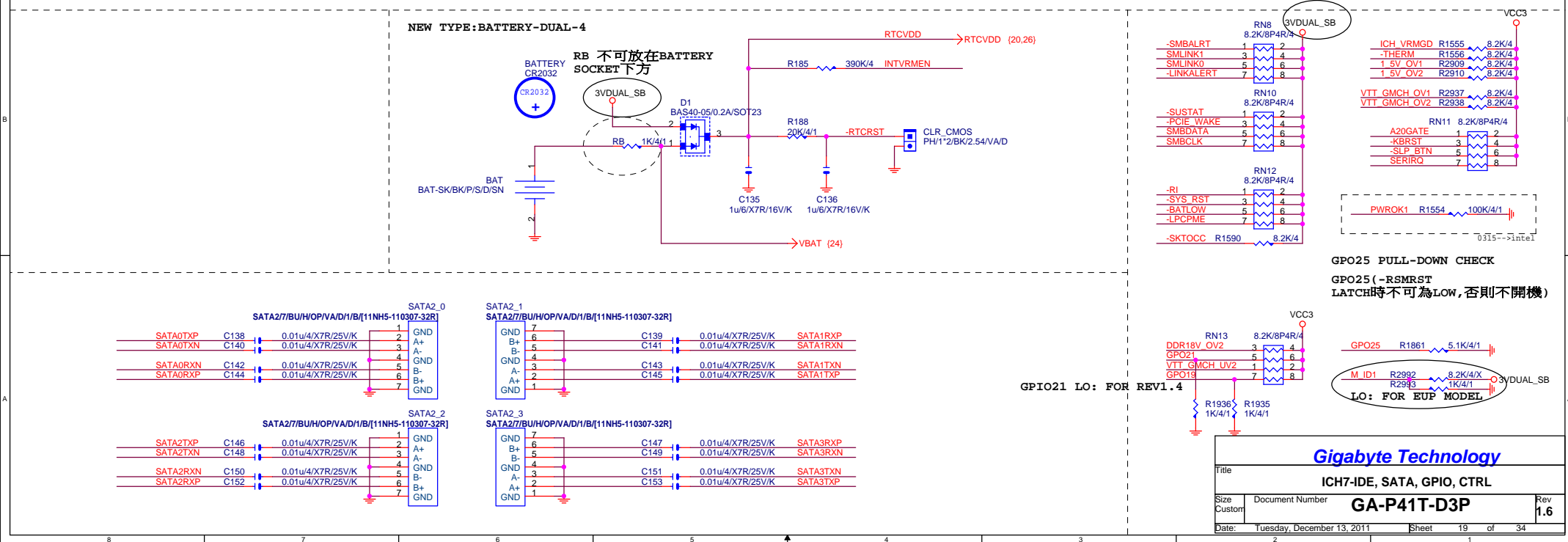
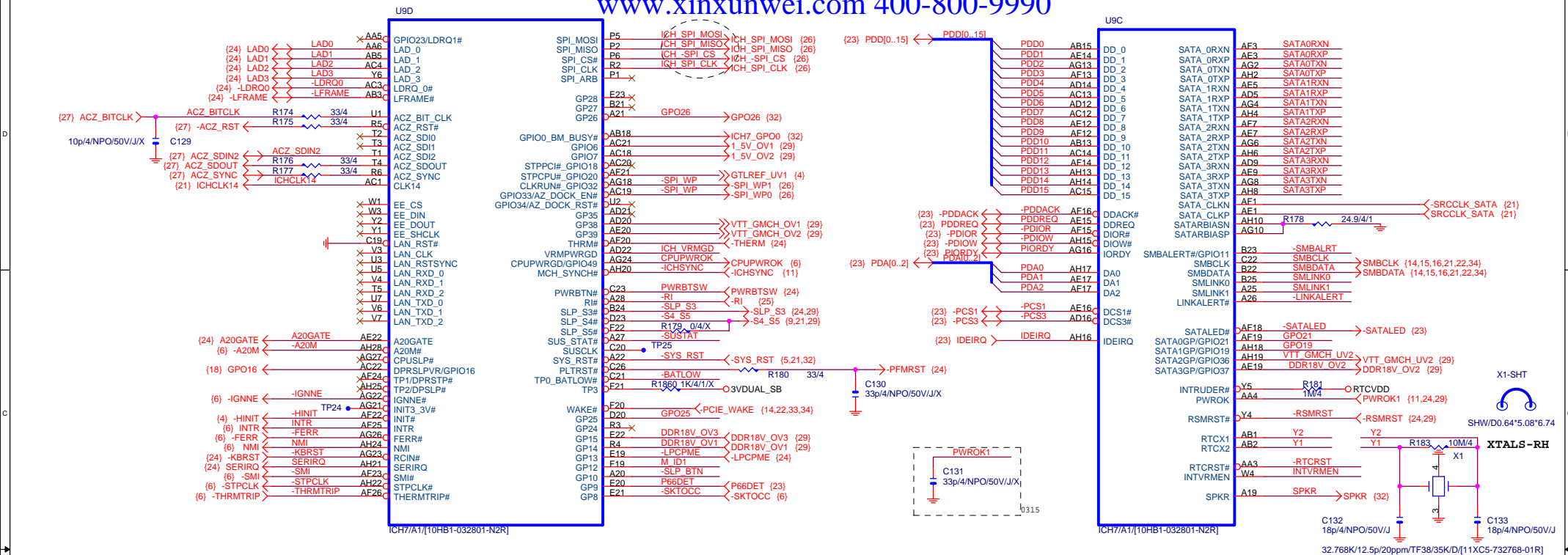
ICH7 ONLY 4 LANE

VCC1_5 R173 24.9/4/1 C25 DMI_ZCOMP
D25 DMI_IRCOMP

{21} -SRCCLK_ICH	}	-SRCCLK_ICH	AE28
{21} SRCCLK_ICH		SRCCLK_ICH	AE27

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Title			
ICH7-PCI, DMI, LAN, USB			
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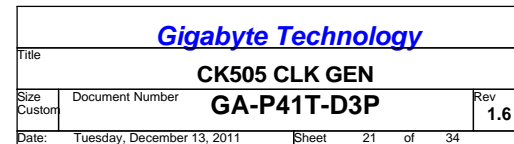




ICH7-PWR & GND

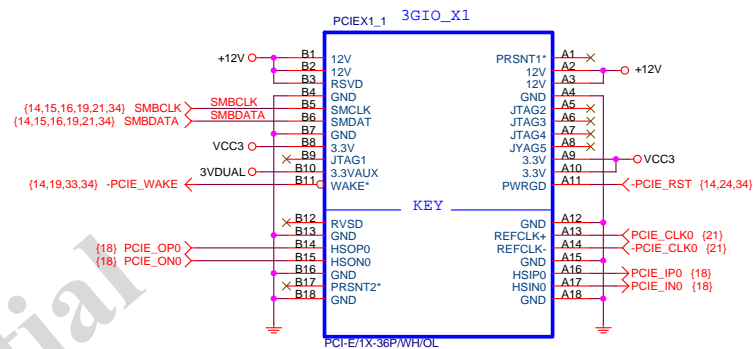
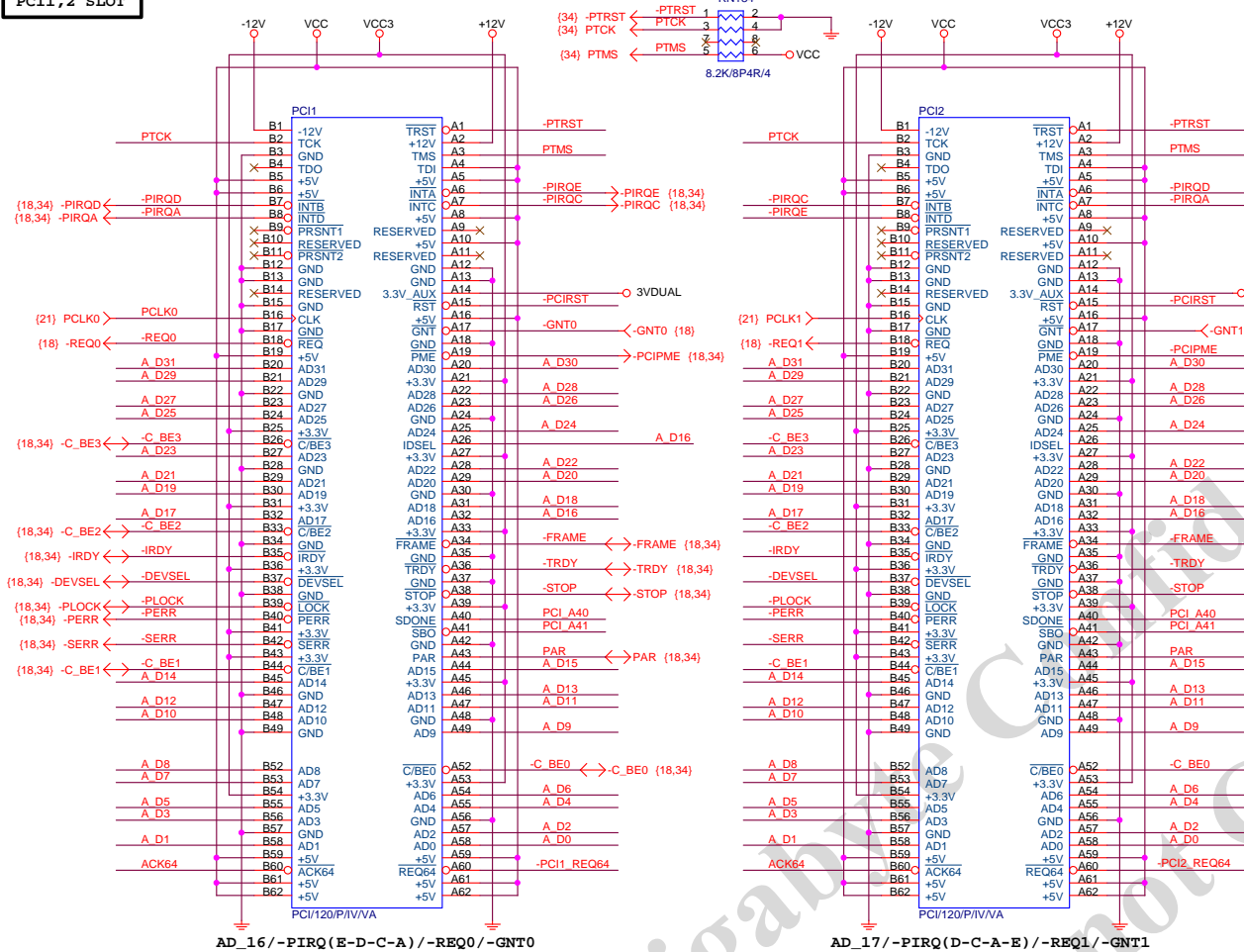
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PCI1,2 SLOT

P41T*1



(18,34) A_D[0..31] ↔ A_D[0..31]

-PCIRST ↔ -PCIRST (18,34)

C208
33p/4/NPO/50V/J/X

Place close to PCI1

(18) -REQ4 ↔ -REQ4

(18) -REQ3 ↔ -REQ3

(18) -REQ1 ↔ -REQ1

(18,34) -REQ2 ↔ -REQ2

(18) -REQ0 ↔ -REQ0

(18,34) PAR ↔ PAR

(18) -REQ5 ↔ -REQ5

ACK64 (34)

ACK64 (34)

ACK64 (34)

ACK64 (34)

-FRAME ↔ -FRAME

-TRDY ↔ -TRDY

-DEVSEL ↔ -DEVSEL

-STOP ↔ -STOP

-PLOCK ↔ -PLOCK

-PERR ↔ -PERR

-SERR ↔ -SERR

(18,34) -PIRQC ↔ -PIRQC

(18,34) -PIRQD ↔ -PIRQD

(18,34) -PIROA ↔ -PIROA

(18) -PIROB ↔ -PIROB

(18,34) -PIRQE ↔ -PIRQE

(18) -PIROF ↔ -PIROF

(18) -PIROH ↔ -PIROH

(18) -PIROG ↔ -PIROG

BC91
0.1u/4/X7R/16V/K/X

BC93
0.1u/4/X7R/16V/K/X

BC95 0.1u/4/X7R/16V/K/X

BC96 0.1u/4/X7R/16V/K/X

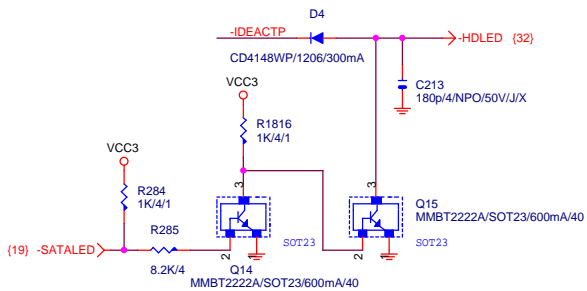
BC97 0.1u/4/X7R/16V/K/X

EC29 560u/FP/D.6/3V/68/8m

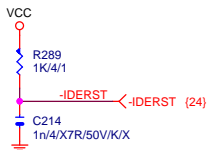
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Title					PCI SLOT 1, 2/PCIEX1					Rev		
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Custom												
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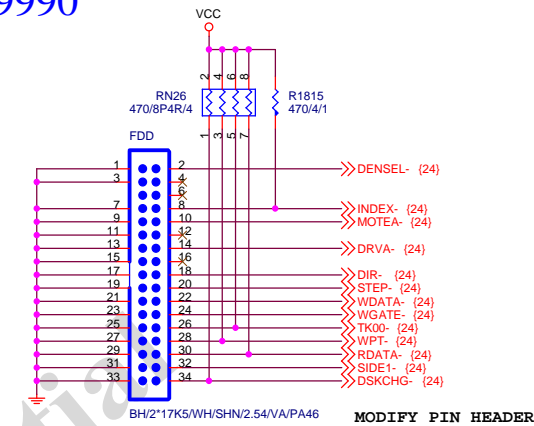
IDE/SATA LED



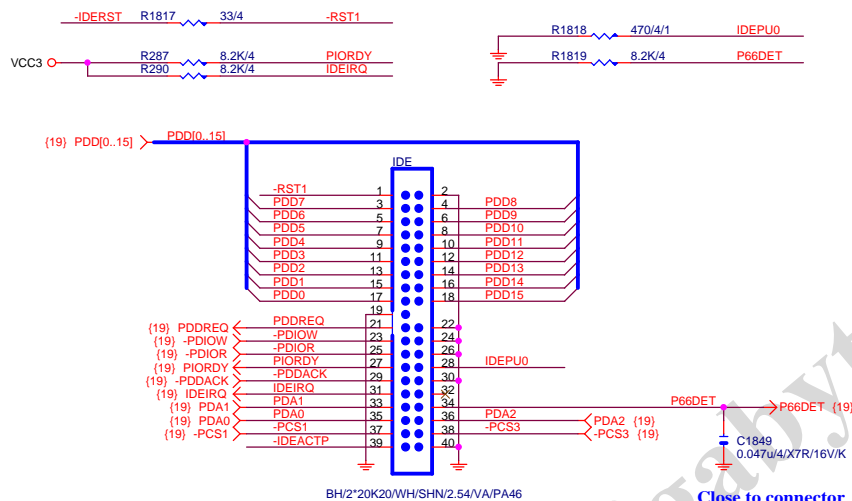
IDE RESET



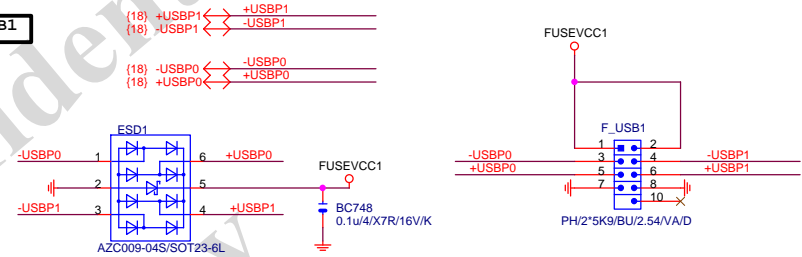
FLOPPY



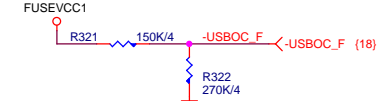
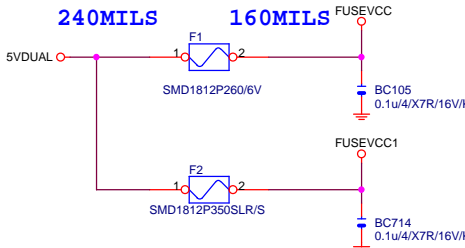
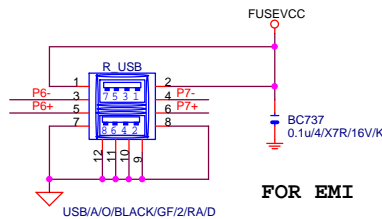
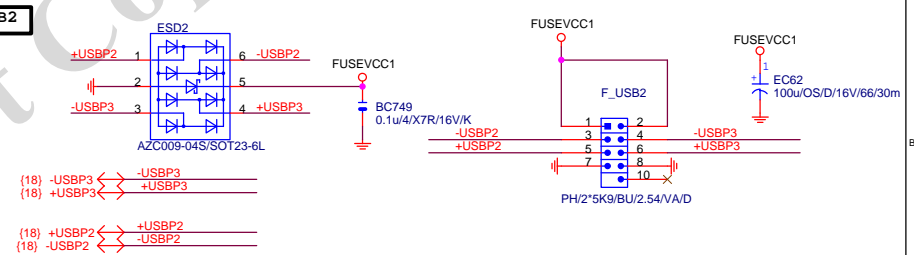
IDE



FRONT USB1

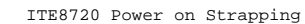


FRONT USB2

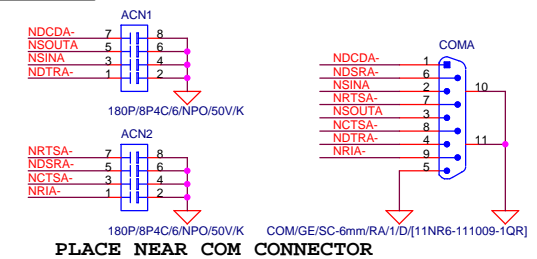
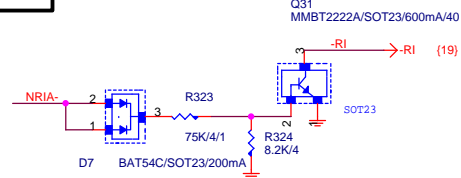
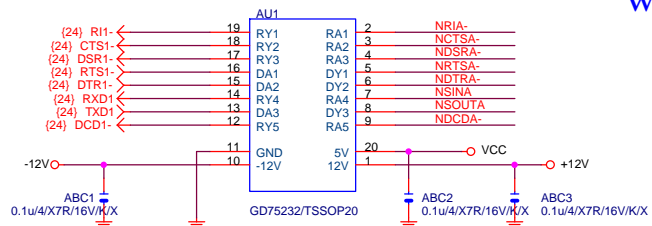


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IDE,FDD,F_USB		
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JP2	1	Disable VID/SVID output pins
	0	Enable VID00~7 output pins
JP3	1	SPI-Flash Disable
	0	SPI-Flash Enable
JP4	1	k8 power sequency function is Disable
	0	k8 power sequency function is Enable
JP5	1	Disable WDT reset PWROK
	0	Enable WDT reset PWROK
JP6	1	Parallel VID output
	0	Serial VID output
JP7	1	Enable Dual BIOS Function
	0	Disable Dual BIOS Function



(24) PD[0..7] ↔ PD0..7

(24) STB- ↔ STB- 5 6 LPT1

(24) AFD- ↔ AFD- 1 2 LPT14

PD0 3 4 LPT2

(24) INIT- ↔ INIT- 7 8 LPT16

33/8P4R/4

PRN2

PD3 3 4 LPT5

PD2 1 2 LPT4

PD1 5 6 LPT3

(24) SLIN- ↔ SLIN- 7 8 LPT17

33/8P4R/4

PRN5

PD6 1 2 LPT8

PD7 3 4 LPT9

PD4 5 6 LPT6

PD5 7 8 LPT7

33/8P4R/4

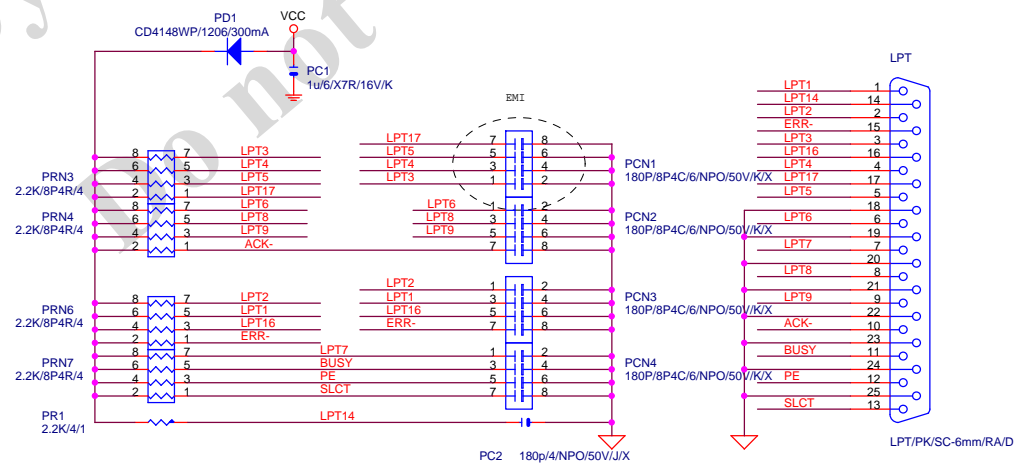
(24) ERR- ↔ ERR-

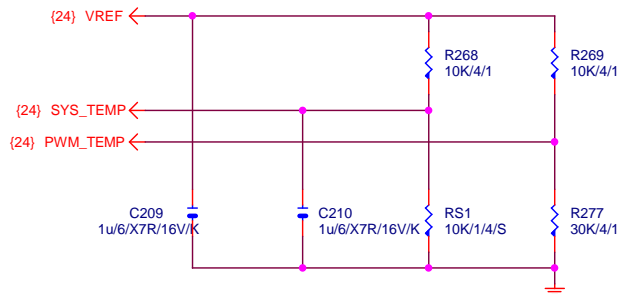
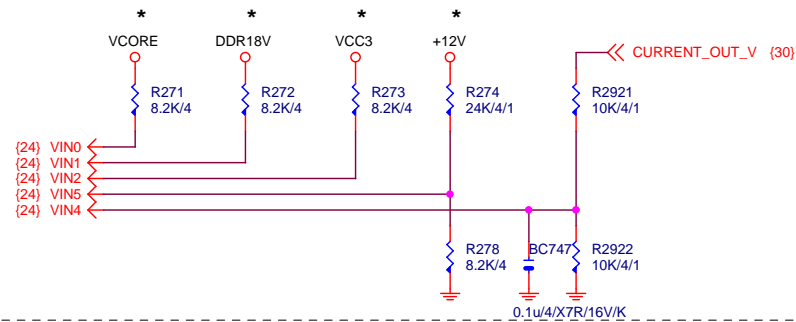
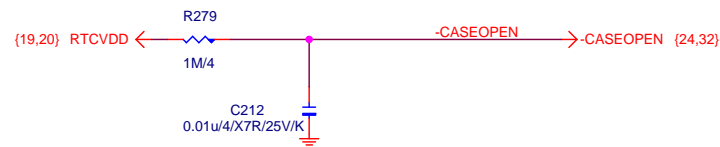
(24) ACK- ↔ ACK-

(24) BUSY- ↔ BUSY-

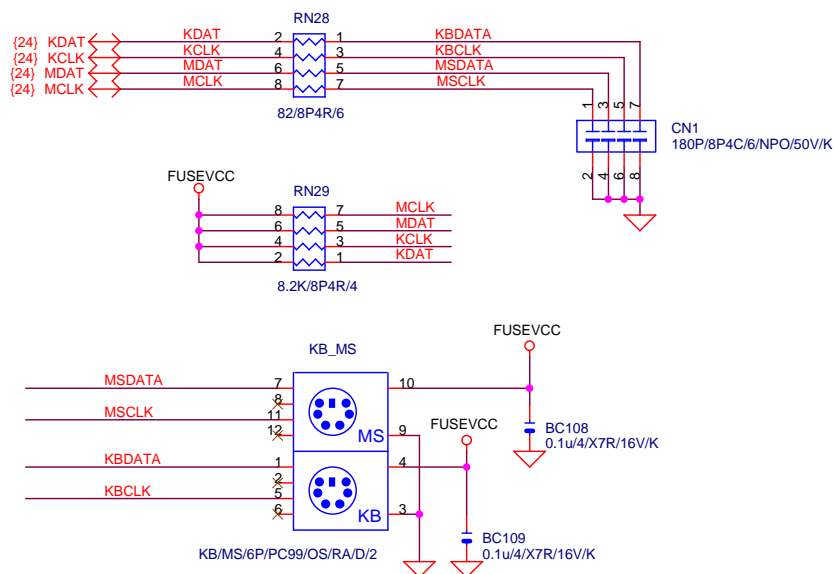
(24) PE ↔ PE

(24) SLCT ↔ SLCT

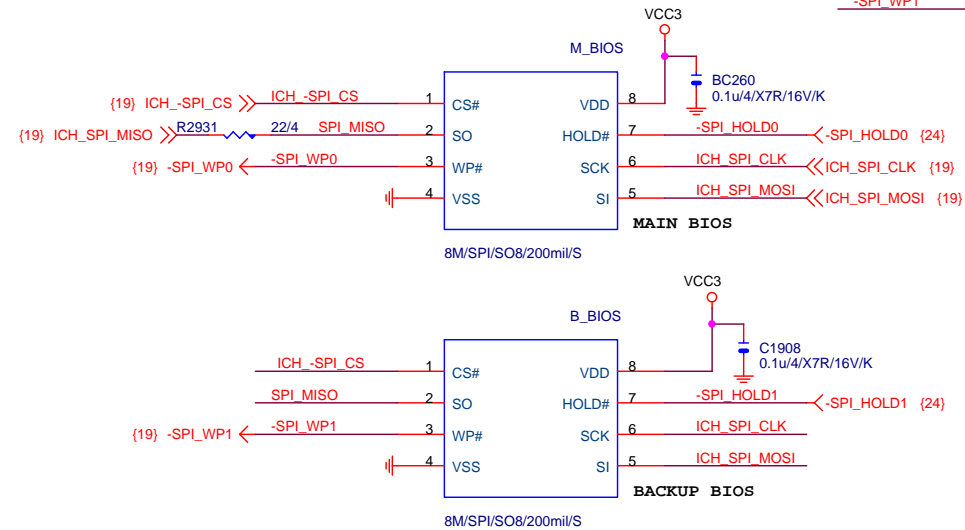
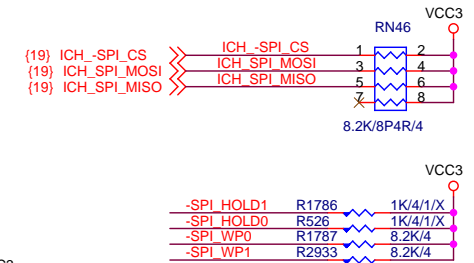


TEMP H/W MONITOR**VOLTAGE-- H/W MONITOR****CASE OPEN**

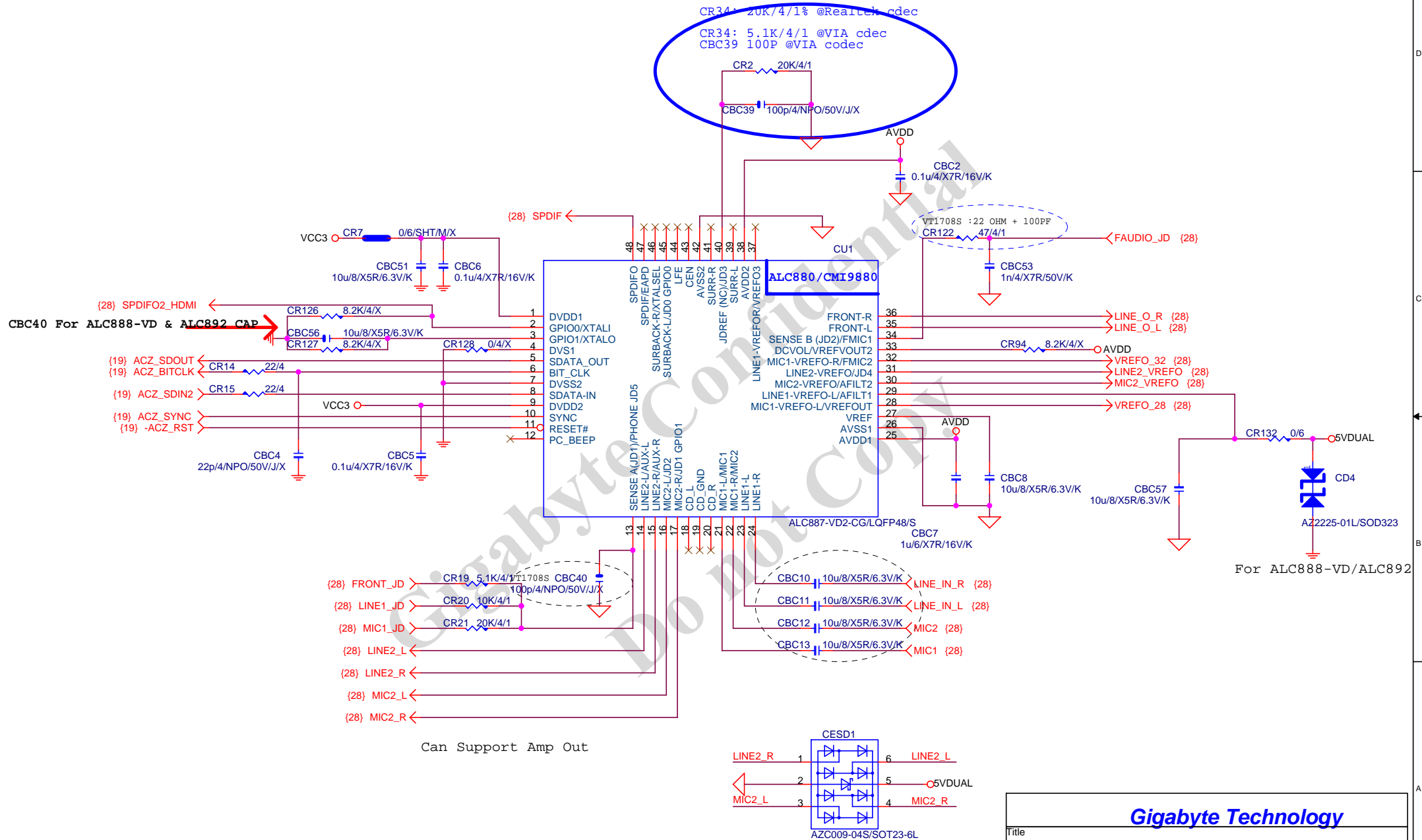
Case Open Circuits

KB/MS**DUAL BIOS**

(NEW HOLD# DESIGN)

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HW-MONITOR/CI/KB/MS/BIOS		
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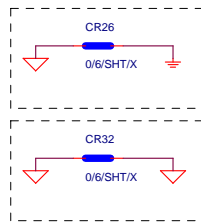
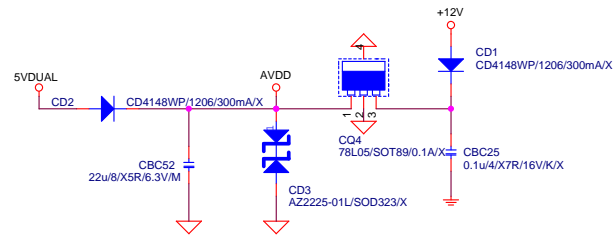
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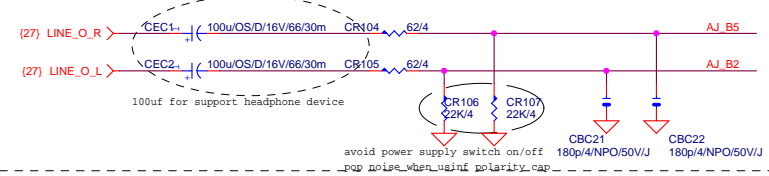
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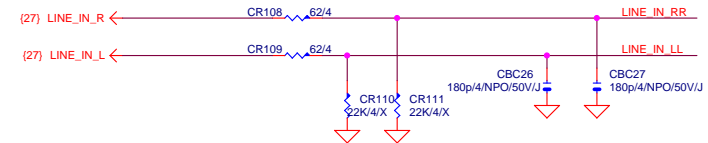
CODEC POWER/EMI PAD



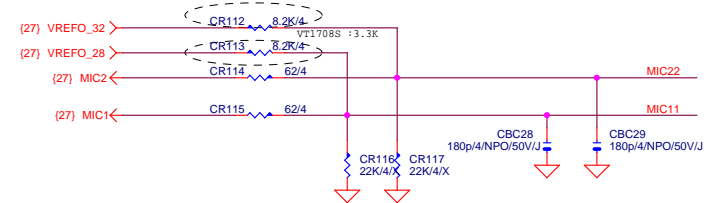
LINE-OUT 4



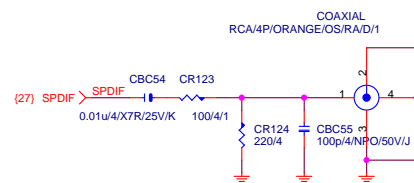
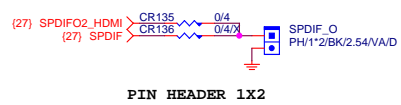
LINE-IN



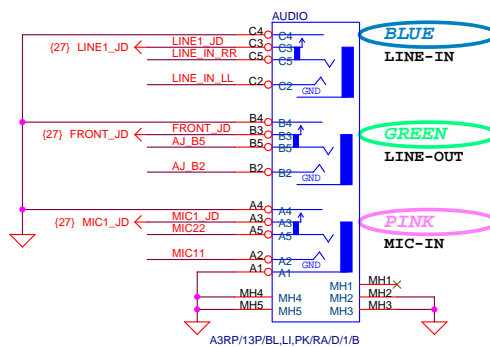
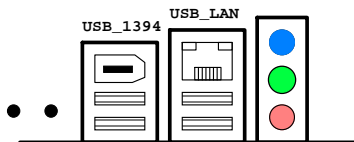
MIC-IN



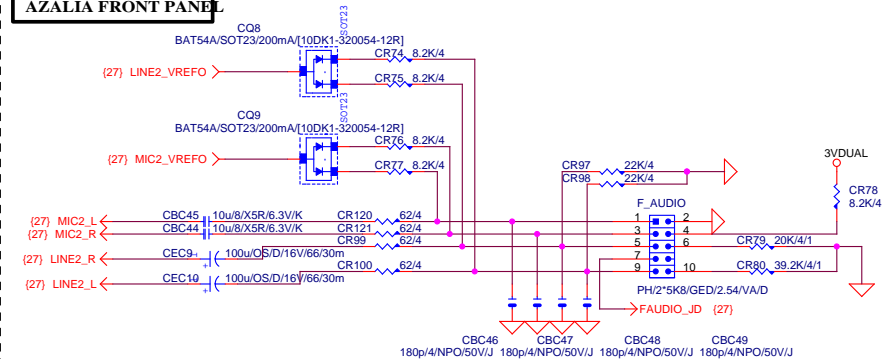
SPDIF



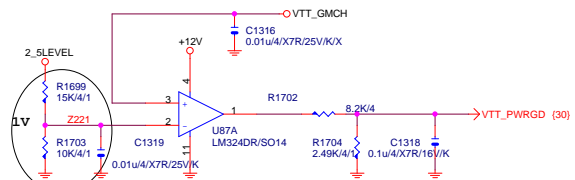
AZALIA JACK



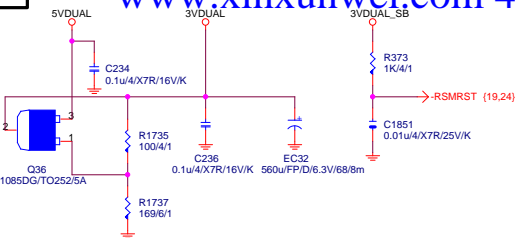
AZALIA FRONT PANE



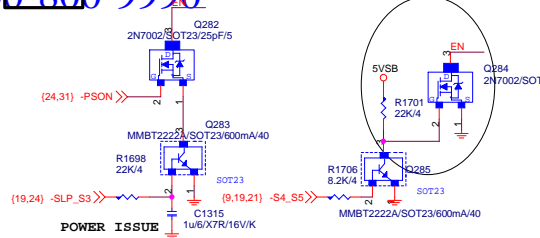
VTT_PWRGD



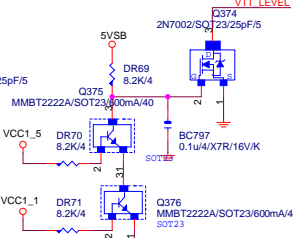
3VDUAL



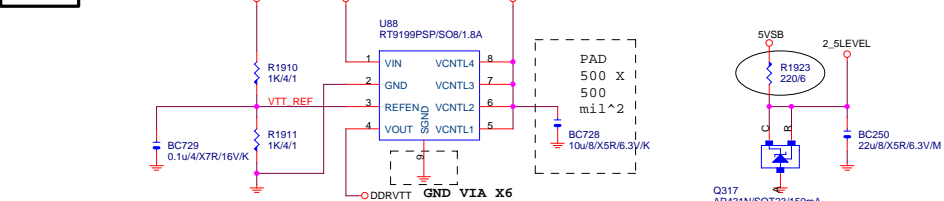
VTT_PWRGD



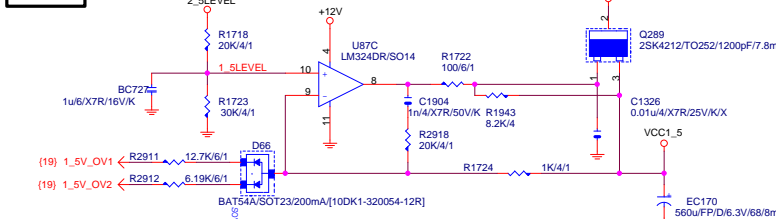
FOR NON-CPU CAN SHUT-DOWN



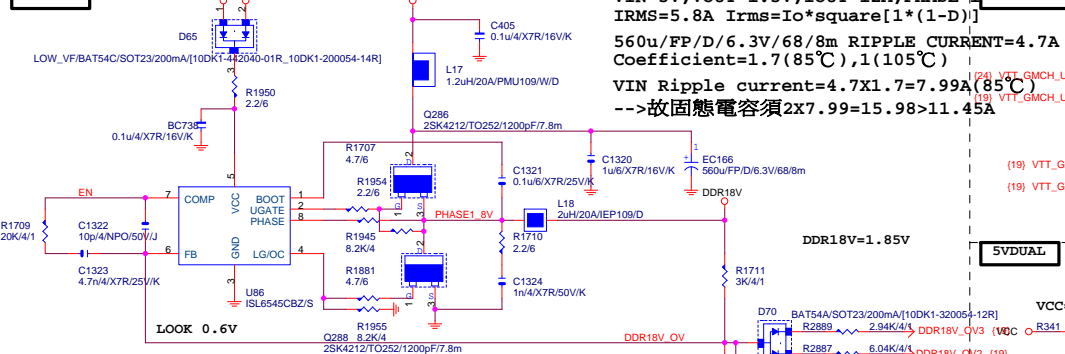
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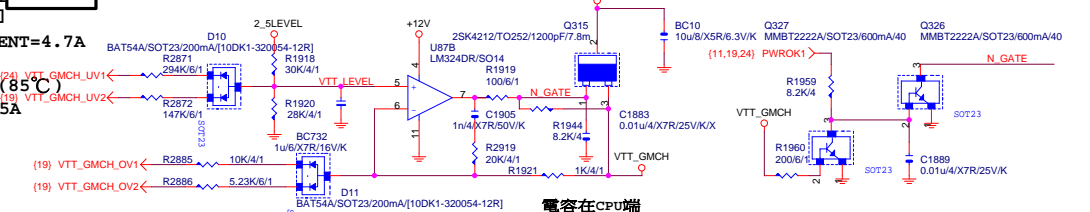
VCC1_5



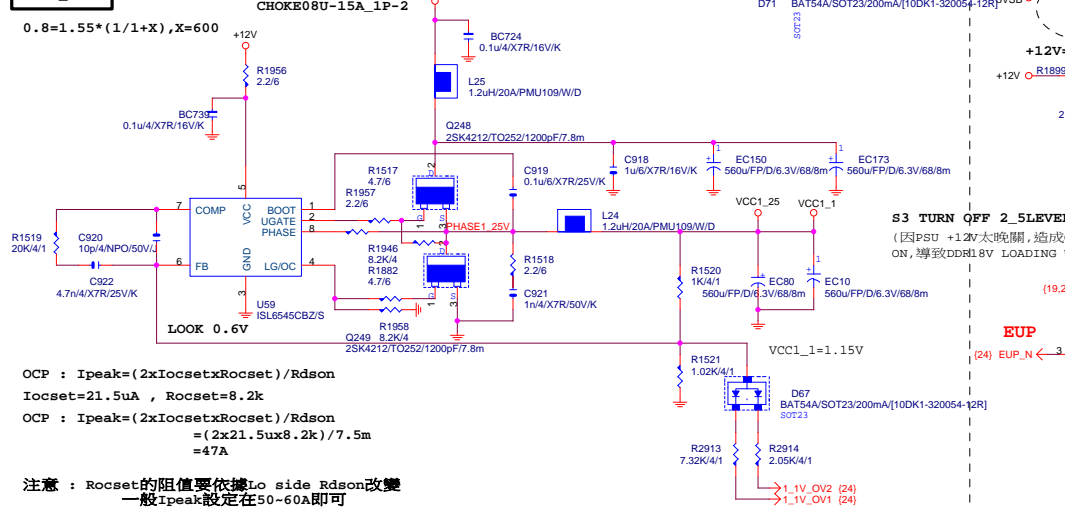
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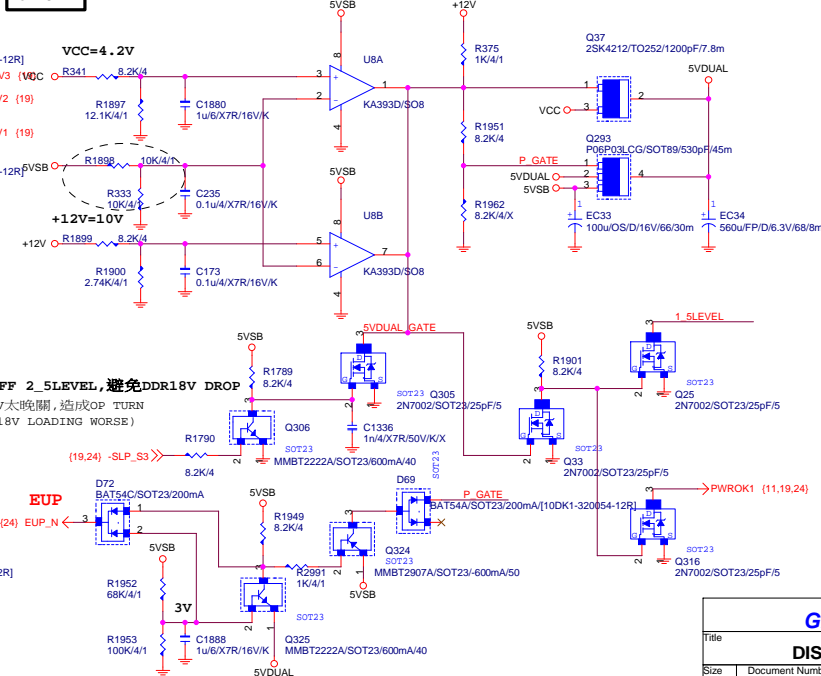
VTT_GMCH



VCC1_25



5VDUAL



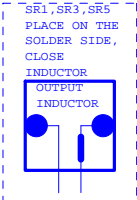
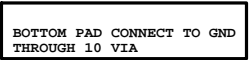
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DISCRETE POWER / FAN CTRL

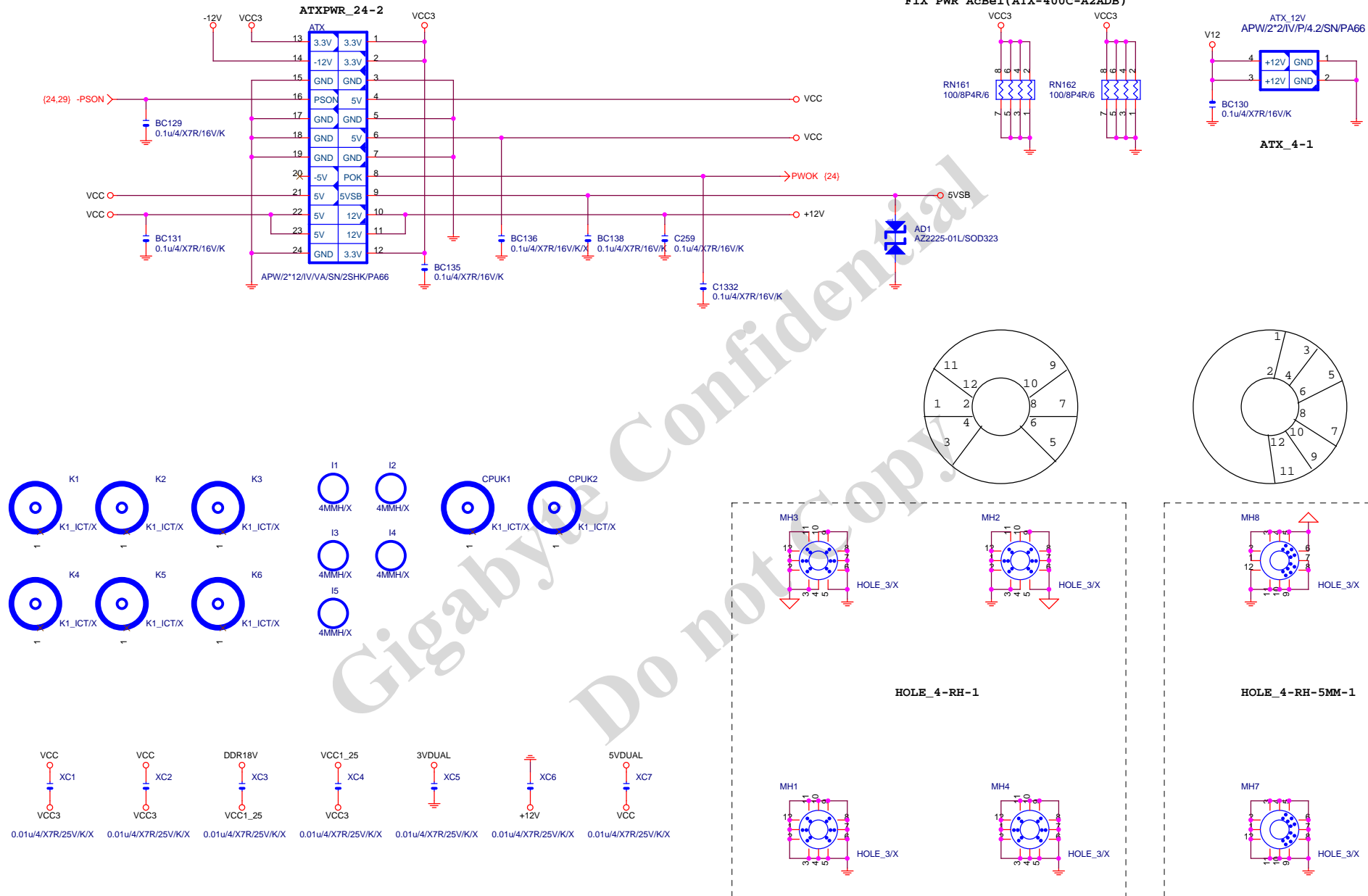
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ATX POWER CONNECTOR

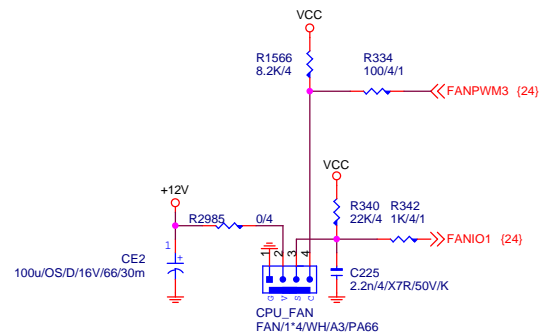


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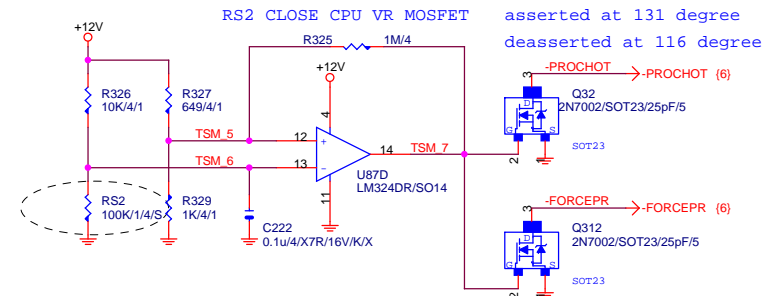
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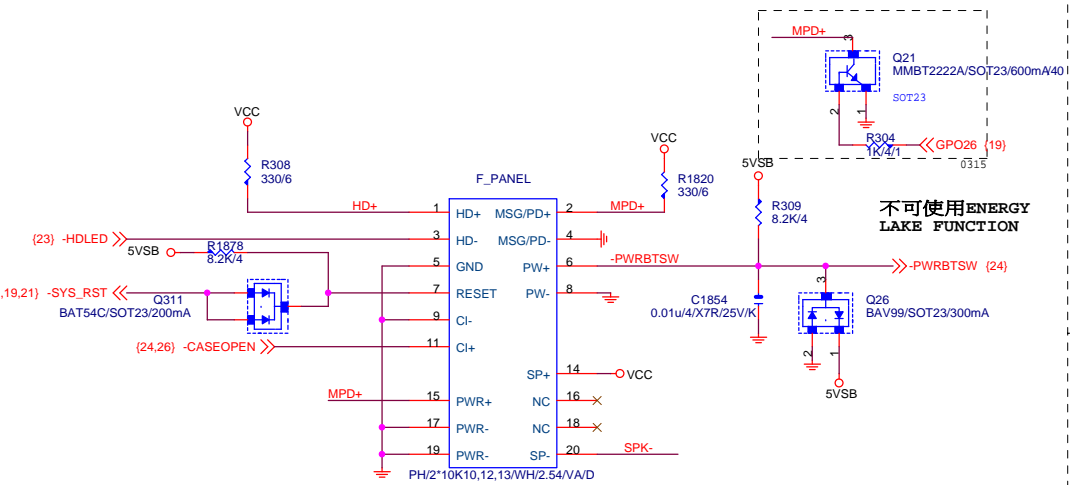
CPU SMART FAN SMART FAN



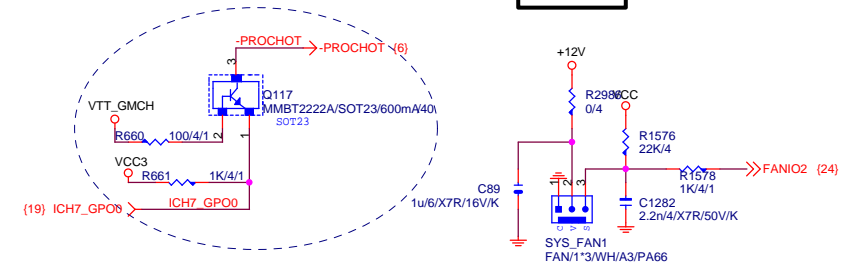
PROCESSOR HOT



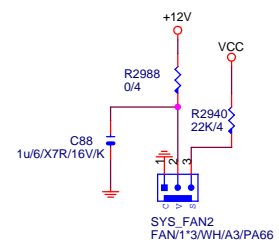
INTEL FRONT PANEL



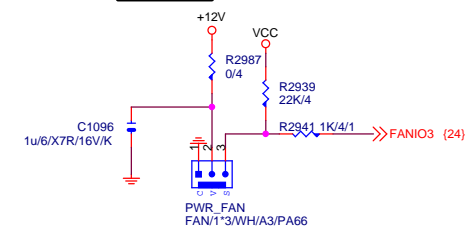
SYS_FAN1



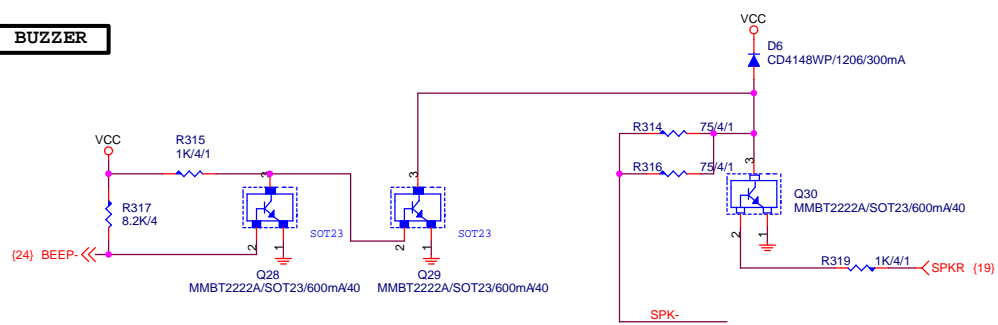
SYS_FAN2



PWR FAN



BUZZER



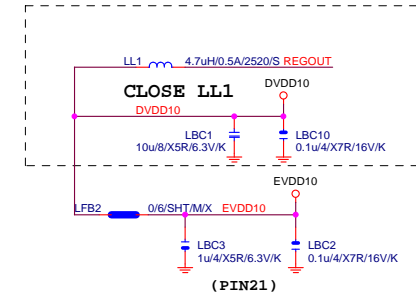
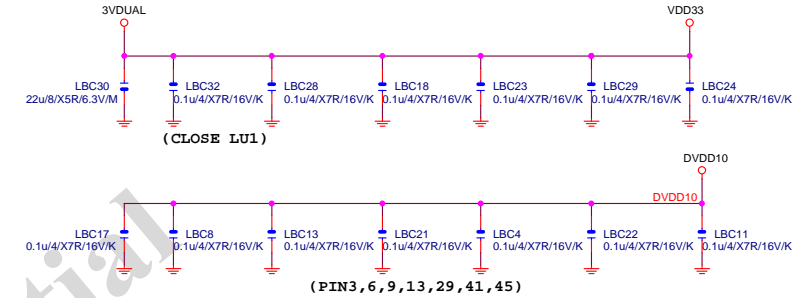
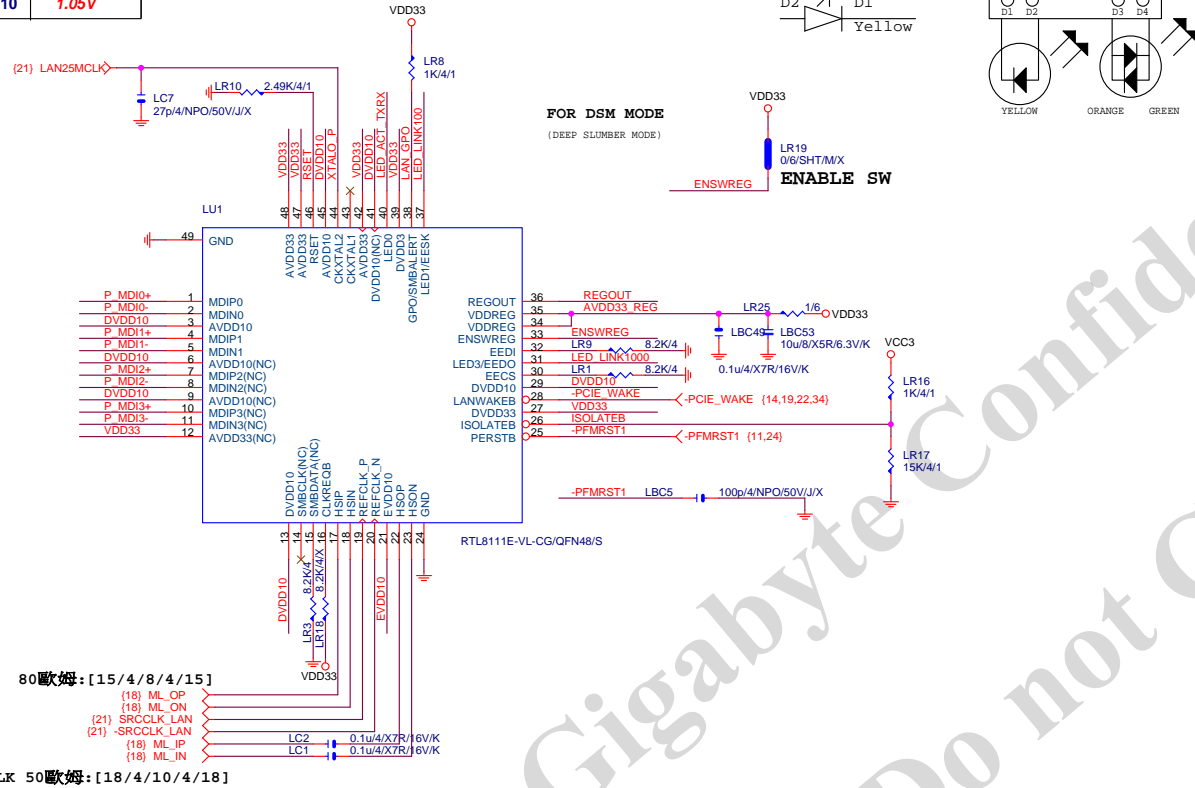
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FRONT PANEL / FAN CTRL			
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PCIE-1G LAN

Power domain chart

	RTL8111E
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V



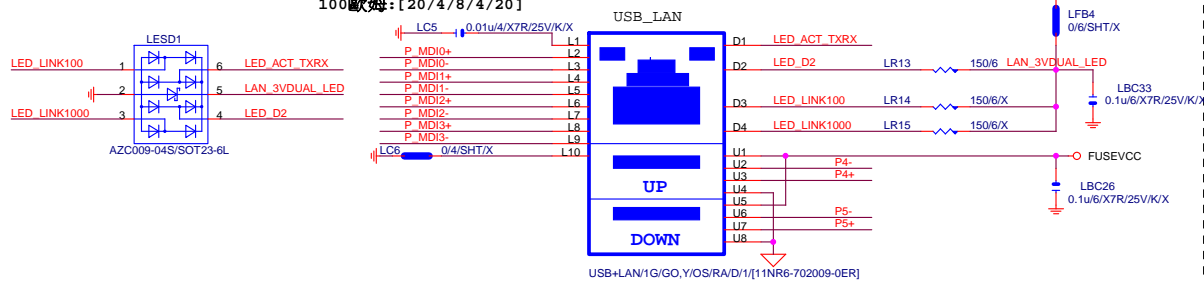
USB_LAN CONNECTOR

RTL8101E : L1+L10-->AVDD18+0.1u(BIOS DISABLE MDI-X FUNCTION)

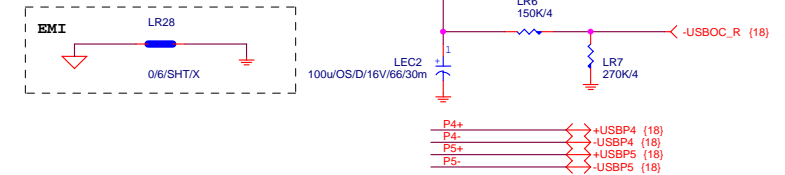
1G : USB+LAN/1G/GO,Y/OS/RA/D/1

100M: USB+LAN/100/GO,Y/OS/RA/D/1

100欧姆:[20/4/8/4/20]



USB_LAN



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